REMARKS/ARGUMENTS

The foregoing amendment and the following arguments are provided to impart precision to the claims, by more particularly pointing out the invention, rather than to avoid prior art.

35 U.S.C. § 102(b) Rejections

Examiner rejected claims 1-11, 13-19 and 21-30 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 6,085,330 (hereinafter "Hewitt").

> To anticipate a claim, the reference must teach every element of the claim. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." (Manual of Patent Examining Procedures (MPEP) ¶ 2131.)

Applicant's independent claims 1, 13, 21 and 27 of the present application includes limitations not disclosed or taught by the Hewitt. As a result, applicant's claims 1, 13, 21 and 27 are not anticipated by Hewitt.

For example, applicant's independent claims1 and 13 includes the limitation, or similar thereto, of:

> a controller to snoop the cache via the first bus interface during a first mode of operation and to snoop the cache via the second bus interface during a second mode of operation, the second mode of operation being a lower power mode than the first mode of operation, and the first bus interface to be powered down during the second mode of operation, ~~wherein~~ the first bus interface is coupled to the controller via a first bus, the first bus is a parallel bus, and the second bus is a serial bus having a single data line, the first bus being wider than the second bus, the first bus to consume more power during the first mode of operation than the second bus consumes during the second mode of operation; and

a main memory and a peripheral device, the peripheral device to request an access of the main memory via the controller.

Applicant's independent claim 21 includes the limitations, or similar thereto, of:

a low power bus interface through which the memory region may be snooped during a low power mode of operation, the high power bus interface is to be powered down during the low power mode of operation, and the high power bus interface supports a first bus, and the low power bus interface supports a second bus that is narrower than the first bus, the low power bus interface provides for source-synchronous operation and the high power bus interface lacks support for source-synchronous operation; and
a memory bus interface.

Applicant's independent claim 27 includes the limitations, or similar thereto, of:

snooping a cache via a high power parallel bus during a high power mode of operation;
transitioning to a low power mode of operation, including powering down the high power bus and flushing a cache; and
snooping the cache via a low power serial bus having a single data line during a low power mode of operation, including providing a clock signal to the cache via the low power bus.

Hewitt does not disclose the limitations added to applicant's independent claims 1, 13, 21, nor 27. Therefore, as a result of Hewitt not disclosing applicant's claimed limitation, applicant's independent claims are not anticipated by Hewitt.

Furthermore, the remaining claims depend from at least one of the independent claims as discussed above, and therefore also include the

distinguishing claim limitations. As a result, applicant's remaining dependent claims are also not anticipated by Hewitt.

CONCLUSION

Applicants respectfully submit the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call John Ward at (408) 720-8300, x237.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

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